

WHAT IS CLAIMED IS:

1 1. A process for forming a pattern comprising:
2 a resist pattern formation step of coating a first resist
3 film and a second resist film in order on a film to be etched
4 on a substrate, and further, forming a resist pattern by
5 patterning said first resist film and said second resist film
6 to make said first resist film broader than said second resist
7 film while making said second resist film positioned on said
8 first resist film;

9 a first patterning step of etching said film to be etched
10 to form a first pattern in said film to be etched by using said
11 resist pattern as a mask; and

12 a resist etching step of etching said resist pattern to
13 remove remaining resist pattern at least a portion of said first
14 resist film, said portion being not covered by said the second
15 resist film, to thereby form a remaining resist pattern
16 consisting of said first resist film and said second resist
17 film, said resist etching step further being constructed such
18 that said second resist film is in a state of a resist film
19 having higher resistance against dry-etching than that of said
20 first resist film at least during said resist etching step.

1 2. The process for forming a pattern according to claim
2 1, wherein said resist pattern includes a first opening formed
3 in said first resist film and a second opening formed in said
4 second resist film in said resist pattern formation step, said
5 first opening is formed inside said second opening, and said
6 remaining resist pattern is formed to have an overhang of said

100448500 "205220" 205220

7 second resist film with respect to said first resist film in
8 said resist etching step.

1 3. The process for forming a pattern according to claim
2 1, wherein said second resist film is coated as a resist film
3 having higher resistance against an etchant used in said resist
4 etching step than that of said first resist film in said resist
5 pattern formation step of coating said first resist film and
6 said second resist film.

1 4. The process for forming a pattern according to
2 claim 1, wherein said resist pattern is subjected to a plasma
3 treatment step to modify said second resist film using a plasma
4 treatment gas to change said second resist film into a modified
5 resist film having higher resistance against dry-etching than
6 that of said first resist film between said first patterning
7 step and said resist etching step.

1 5. The process for forming a pattern according to claim
2 4, wherein said plasma treatment step employs one of a gas
3 containing an O₂ gas, a gas containing a fluorine series gas
4 and a gas containing a mixture of an O₂ gas and a fluorine series
5 gas, as said plasma treatment gas.

1 6. The process for forming a pattern according to claim
2 4, wherein said resist etching step is further constructed such
3 that said second resist film is made to include silicon atoms
4 to change said second resist film into a silicon-doped second
5 resist film and then, said silicon-doped second resist film
6 is modified to a silicon oxide film through said plasma treatment
7 step using a mixed gas containing at least oxygen.

1 7. The process for forming a pattern according to claim
2 6, wherein said second resist film previously consists of a
3 resist film capable of being silylated and between said first
4 patterning step and said plasma treatment step, a silylating
5 step of immersing said first resist film and said second resist
6 film in a silylating agent containing silazane to silylate only
7 said second resist film is carried out.

1 8. The process for forming a pattern according to claim
2 1, wherein said second resist film is modified to a modified
3 resist film having higher resistance against dry-etching than
4 that of said first resist film, while removing at least a portion
5 of said first resist film, said portion being not covered by
6 said second resist film, in said resist etching step.

1 9. The process for forming a pattern according to claim
2 1, wherein a second patterning step of etching said film to
3 be etched to form a second pattern in said film to be etched
4 is carried out by using said remaining resist pattern as a mask
5 after said resist etching step.

1 10. The process for forming a pattern according to claim
2 1, wherein a gate wiring and a gate insulating film covering
3 said gate wiring are formed on said substrate and under said
4 film to be etched, said film to be etched is a laminated film
5 formed by depositing a semiconductor film, a semiconductor film
6 doped with impurities and a metal film for source/drain
7 electrodes in order on said gate insulating film, and said resist
8 pattern is formed on said laminated film.

1 11. The process for forming a pattern according to claim
2 10, wherein said resist pattern is formed such that a resist

20250420 09:25:02

3 film out of said resist pattern, said resist film consisting
4 of only said first resist film, is positioned above a
5 later-formed channel region of a thin film transistor, at least
6 said metal film for source/drain electrodes is etched and removed
7 to form an electrode pattern made of said metal film for
8 source/drain electrodes in said step of subjecting said film
9 to be etched to said first patterning step by using said resist
10 pattern as a mask, said resist pattern is etched to remove only
11 said resist film consisting of only said first resist film to
12 make said resist pattern become said remaining resist pattern
13 in said resist etching step, and after said resist etching step,
14 a second patterning step of etching and removing said metal
15 film for source/drain electrodes, said semiconductor film doped
16 with impurities and a part of said semiconductor film by using
17 said remaining resist pattern as a mask to form a channel region
18 of said thin film transistor in said laminated film is performed.

1 12. The process for forming a pattern according to claim
2 10, wherein a common electrode is formed together with said
3 gate wiring to have comb-shaped electrodes and in said resist
4 pattern formation step, said resist pattern consisting of said
5 first resist film and said second resist film is formed on said
6 metal film for source/drain electrodes to cover a later-formed
7 pixel electrode, said later-formed pixel electrode being
8 interposed between said comb-shaped electrodes of said common
9 electrode.

1 13. The process for forming a pattern according to claim
2 10, wherein said second resist film is coated as a resist film
3 having higher resistance against an etchant used in said resist

4 etching step than that of said first resist film in said resist
5 pattern formation step.

1 14. The process for forming a pattern according to claim
2 11, wherein a plasma treatment step of modifying remaining resist
3 pattern said second resist film out of said resist pattern to
4 a modified resist film having higher resistance against
5 dry-etching than that of said first resist film is performed
6 between said first patterning step and said resist etching step.

1 15. The process for forming a pattern according to claim
2 14, wherein said modified resist film is formed such that said
3 second resist film is made to include silicon atoms to change
4 said second resist film into a silicon-doped second resist film
5 and then, said silicon-doped second resist film is modified
6 to a silicon oxide film through said plasma treatment step
7 performed using a mixed gas containing at least oxygen.

1 16. The process for forming a pattern according to claim
2 11, wherein said process for forming a pattern further comprises
3 after said second patterning step:

4 a step of removing said remaining resist pattern used
5 to form said channel region of said thin film transistor and
6 subsequently, depositing a protective insulating film covering
7 said gate insulating film;

8 a step of coating a third resist film and a fourth resist
9 film in order on said protective insulating film and patterning
10 said third resist film and said fourth resist film to make said
11 third resist film broader than said fourth resist film while
12 making said fourth resist film positioned on said third resist
13 film to form a second resist pattern consisting of said third

20250408 09:00:00

14 resist film and said fourth resist film, said second resist
15 pattern having an opening therein;

16 a step of at least removing associated portion of said
17 protective insulating film by using said second resist pattern
18 as a mask to expose a surface of an electrically conductive
19 layer consisting of said laminated film and positioned under
20 said protective insulating film; and

21 a step of selectively etching said third resist film out
22 of said second resist pattern to make an overhang of said fourth

23 resist film with respect to said third resist film in said opening,

24 wherein said overhang is formed such that said fourth
25 resist film is made to include silicon atoms to change said
26 fourth resist film into a silicon-doped fourth resist film and
27 then, said silicon-doped fourth resist film is modified to a
28 silicon oxide film through a plasma treatment performed using
29 a mixed gas containing at least oxygen, and thereafter, an
30 associated part of said third resist film is removed in a lateral
31 direction.

1 17. The process for forming a pattern according to claim
2 16, wherein an electrically conductive material is deposited
3 on a surface consisting of said second resist pattern, said
4 protective insulating film and said electrically conductive
5 layer, and said second resist pattern is removed together with
6 said electrically conductive material thereon to leave said
7 electrically conductive material in and around said opening
8 after forming said overhang.